MC14503B

Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non−inverting buffer with 3−state outputs, and a high current source and sink capability. The 3−state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

Features

- 3−State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097
- These Devices are Pb−Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	− 0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	− 0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	±10	mA
Output Current (DC or Transient) per Pin	I_{out}	±25	mA
Power Dissipation, per Package (Note 2)	P_D	500	mW
Ambient Temperature Range	T_A	− 55 to +125	°C
Storage Temperature Range		− 65 to +150	°C
Lead Temperature (8−Second Soldering)		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
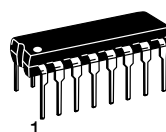
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
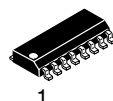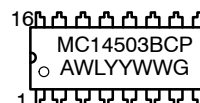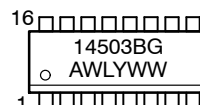
ON Semiconductor®

MARKING DIAGRAMS

PDIP−16
P SUFFIX
CASE 648

16
MC14503BCP
AWLYYWWG
1

SOIC−16
D SUFFIX
CASE 751B

16
14503BG
AWLYWW
1

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.
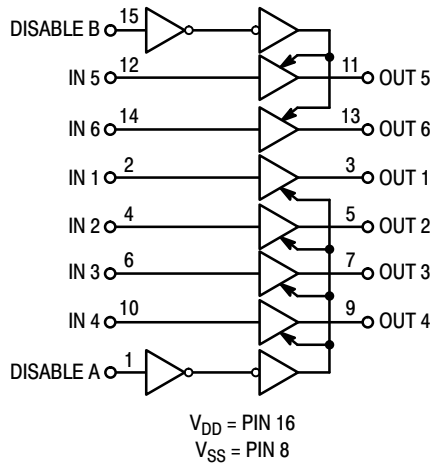
MC14503B

PIN ASSIGNMENT

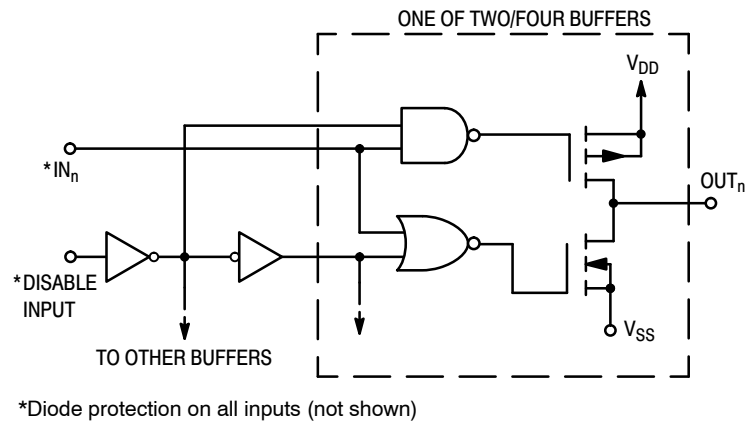|			
DIS A	1 ●	16	V_{DD}
IN 1	2	15	DIS B
OUT 1	3	14	IN 6
IN 2	4	13	OUT 6
OUT 2	5	12	IN 5
IN 3	6	11	OUT 5
OUT 3	7	10	IN 4
V_{SS}	8	9	OUT 4
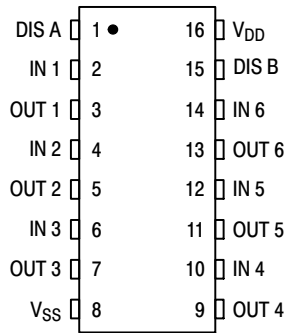
TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

LOGIC DIAGRAM

V_{DD} = PIN 16
V_{SS} = PIN 8

CIRCUIT DIAGRAM

*Diode protection on all inputs (not shown)

ORDERING INFORMATION

Device	Package	Shipping[†]
MC14503BCPG	PDIP−16 (Pb−Free)	500 / Rail
MC14503BDG	SOIC−16 (Pb−Free)	48 / Rail
MC14503BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14503BDR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 3)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = 0		V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
V_{in} = V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage "0" Level (V_O = 3.6 or 1.4 Vdc) (V_O = 7.2 or 2.8 Vdc) (V_O = 11.5 or 3.5 Vdc)		V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
"1" Level (V_O = 1.4 or 3.6 Vdc) (V_O = 2.8 or 7.2 Vdc) (V_O = 3.5 or 11.5 Vdc)		V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	4.5 5.0 5.0 10 15	−4.3 −5.8 −1.2 −3.1 −8.2	− − − − −	−3.6 −4.8 −1.02 −2.6 −6.8	−5.0 −6.1 −1.4 −3.7 −14.1	− − − − −	−2.5 −3.0 −0.7 −1.8 −4.8	− − − − −	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	4.5 5.0 10 15	2.2 2.6 6.5 19.2	− − − −	1.8 2.1 5.5 16.1	2.1 2.3 6.2 25	− − − −	1.2 1.3 3.8 11.2	− − − −	mAdc
Input Current		I_{in}	15	−	± 0.1	−	±0.00001	± 0.1	−	± 1.0	μAdc
Input Capacitance, (V_{in} = 0)		C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current, (Per Package)		I_Q	5.0 10 15	− − −	1.0 2.0 4.0	− − −	0.002 0.004 0.006	1.0 2.0 4.0	− − −	30 60 120	μAdc
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)		I_T	5.0 10 15	I_T = (2.5 μA/kHz) f + I_{DD} I_T = (6.0 μA/kHz) f + I_{DD} I_T = (10 μA/kHz) f + I_{DD}							μAdc
3−State Output Leakage Current		I_{TL}	15	−	± 0.1	−	± 0.0001	± 0.1	−	± 3.0	μAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 pF) + (C_L − 50)$ Vfk where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} − V_{SS}$) in volts, f in kHz is input frequency, and k = 0.006.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ (Note 7)	Max	Unit
Output Rise Time t_{TLH} = (0.5 ns/pF) C_L + 20 ns t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns	t_{TLH}	5.0 10 15	45 23 18	90 45 35	ns
Output Fall Time t_{THL} = (0.5 ns/pF) C_L + 20 ns t_{THL} = (0.3 ns/pF) C_L + 8.0 ns t_{THL} = (0.2 ns/pF) C_L + 8.0 ns	t_{THL}	5.0 10 15	45 23 18	90 45 35	ns
Turn−Off Delay Time, all Outputs t_{PLH} = (0.3 ns/pF) C_L + 60 ns t_{PLH} = (0.15 ns/pF) C_L + 27 ns t_{PLH} = (0.1 ns/pF) C_L + 20 ns	t_{PLH}	5.0 10 15	75 35 25	150 70 50	ns
Turn−On Delay Time, all Outputs t_{PHL} = (0.3 ns/pF) C_L + 60 ns t_{PHL} = (0.15 ns/pF) C_L + 27 ns t_{PHL} = (0.1 ns/pF) C_L + 20 ns	t_{PHL}	5.0 10 15	75 35 25	150 70 50	ns
3−State Propagation Delay Time Output "1" to High Impedance	t_{PHZ}	5.0 10 15	75 40 35	150 80 70	ns
Output "0" to High Impedance	t_{PLZ}	5.0 10 15	80 40 35	160 80 70	ns
High Impedance to "1" Level	t_{PZH}	5.0 10 15	65 25 20	130 50 40	ns
High Impedance to "0" Level	t_{PZL}	5.0 10 15	100 35 25	200 70 50	ns

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
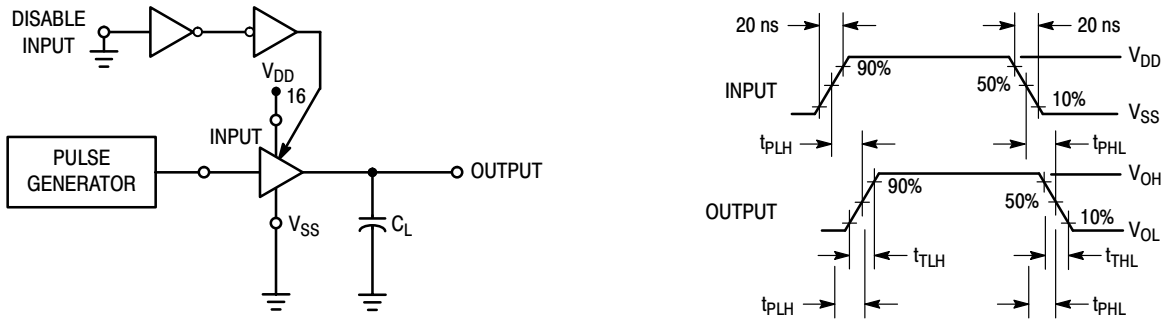
Figure 1. Switching Time Test Circuit and Waveforms
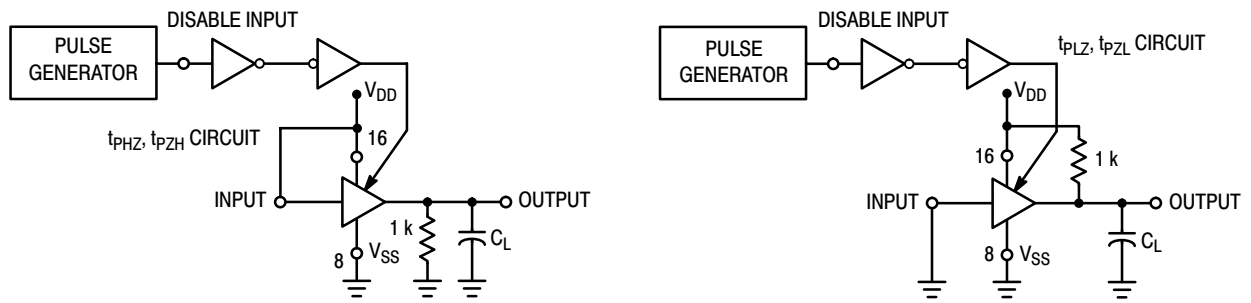(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})
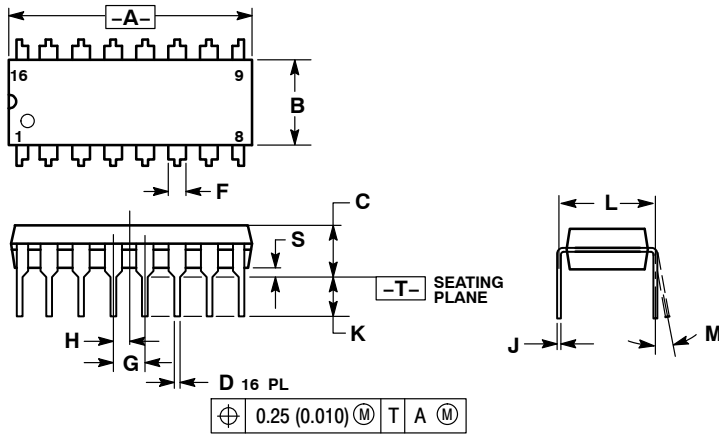
MC14503B
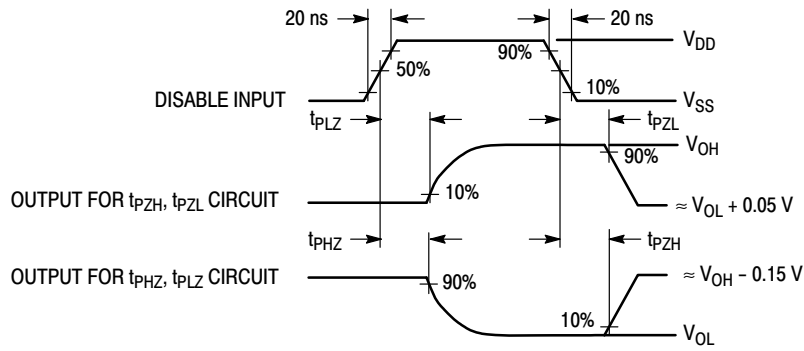
Figure 2. 3−State AC Test Circuit and Waveforms
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})

MC14503B

PACKAGE DIMENSIONS

PDIP−16
CASE 648−08
ISSUE T

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

⊕ | 0.25 (0.010) Ⓜ | T | A Ⓜ

MC14503B

PACKAGE DIMENSIONS

SOIC−16
CASE 751B−05
ISSUE K
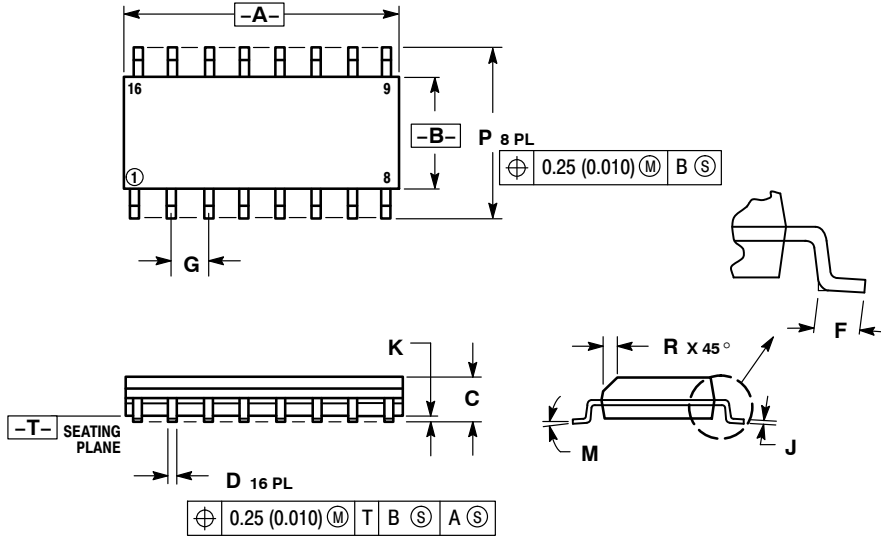
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS